



SE-8065

B. E. - II (Sem. III) (ECC/CO/IT/IC) Examination

May / June - 2011

Digital Logic Design

Time : Hours]

[Total Marks :

Instructions : (1)

नीचे दशांशवले निशानीवाणी विगतो उत्तरवही पर अवश्य लपवी.
 Fillup strictly the details of signs on your answer book.

Name of the Examination :

Name of the Subject :

Subject Code No. : Section No. (1, 2,.....) :

Seat No. :

Student's Signature

- (2) Answer to the sections must be written separate answer book.
- (3) Assume suitable data wherever necessary.
- (4) Figure to the right indicate maximum marks of the question.
- (5) Attempt all questions.

SECTION - I

- Q.1 (a)** Convert the following numbers to decimal 08
- (i) (10001.101)₂
 - (ii) (101011.11101)₂
 - (iii) (0.365)₈
 - (iv) A3E₅
 - (v) CDA₄
 - (vi) (11101.001)₂
 - (vii) B2D₄
 - (viii) (101001011)₂
- (B)** Perform the operation of subtractions with the following binary Numbers using 2's complement 06
- (i) 10010 - 10011 (ii) 100 - 110000 (iii) 11010 - 10000
- (C)** Define 06
- (i) Power dissipation
 - (ii) Propagation delay
 - (iii) Noise margin
- Q.2 (a)** Simplify the Boolean function: 08
- (1) $F(w,x,y,z) = \sum (0,1,2,4,5,6,8,9,12,13,14)$
 - (2) $F(w,x,y) = \sum (0,1,3,4,5,7)$
- (b)** Explain with figures how NAND gate and NOR gate can be used as Universal gate. 07

(b) Simplify the Boolean function:

07

$$(1) F = A'B'C' + B'CD' + A'BCD' + AB'C'$$

$$(2) F = A'B'D' + A'CD + A'BC$$

$$d = A'BC'D + ACD + AB'D' \text{ Where "d" indicates Don't care conditions.}$$

Q – 3 Attempt any Three.

(15)

1. Draw and Explain Full Adder, Implement the circuit with the two half adder.
2. Explain Magnitude Comparator.
3. With logic diagram and truth table explain the working of 3 to 8 line decoder.
4. Design a combinational circuit that generates the 9's complement of a BCD digit .
5. Explain SOP and POS expression using suitable Example.

SECTION - 2

Q-4

A. Do as directed

10

- 1) Give the difference between 'Combination Circuit' and 'Sequential Circuit'.
- 2) Give the Excitation table for J-K Flip Flop.
- 3) In J-K Flip- flop output is _____, when $J = 1, K = 1$.
- 4) Give the excitation table of SR flip flop.
- 5) Give the block diagram of the sequential circuit
- 6) Give the definition of the 'Propagation Delay'.
- 7) In T Flip Flop Output frequency is $\frac{1}{2}$ of its input frequency? **TRUE?FALSE**
- 8) The number of flip flop required to implement mod-7 counter are _____.
- 9) If the clock having frequency 100 Hz is applied to input of the T Flip-Flop output has frequency _____.
- 10) Give the characteristics table of D flip-flop.

B. Attempt the following questions.

1. Explain JK Flip-Flop. Write down logic diagram, characteristics table and Characteristics equation for it. **04**
2. Convert SR Flip-Flop to J-K Flip Flop and SR Flip-Flop to D Flip Flop **06**

Q-5

A. Explain Edge Trigger Flip-Flop in detail.

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B. List the type of the shift register and explain bi-direction shift register.

07

OR

A. What is time race problem? Explain working of the 'Master-Slave' Flip Flop with timing diagram. **07**

B. Explain two bit 'ripple up counter', two bit 'ripple down counter' and two bit 'ripple up/down counter', with timing diagram. **07**

Q.6 Attempt any two

16

A. Explain 'Ring Counter' and 'Twisted Ring Counter' with timing diagram.

B. Write short note on IC Logic Families.

C. Write down applications of Flip-Flop in detail.